QUESTION BANK
DSD– ECE 3rd SEM
CODE: (BTEC-302)

1) Define binary logic?

Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

2) Convert (634) 8 to binary

6 3 4
110 011 100
Ans = 110011100

3) Convert 0.640625 decimal numbers to its octal equivalent.

0.640625 x 8 = 5.125
0.125 x 8 = 1.0
= 0.640 625 10 = **(0.51) 8**

4) Convert 22.64 to hexadecimal number.

16 22 -6
16 1 -1
0
0.64 x 16 = 10.24
0.24 x 16 = 3.84
0.84 x 16 = 13.44
.44 x 16 = 7.04
Ans = (16. A 3 D 7) 16

5) Convert gray code 101011 into its binary equivalent.

Gray Code: 1 0 1 0 1 1
Binary Code: **1 1 0 0 1 0**

6) Subtract (0 1 0 1) 2 from (1 0 1 1) 2

1 0 1 0
0 1 0 1
Answer = 0 1 1 0

7) Add (1 0 1 0) 2 and (0 0 1 1) 2

1 0 1 0
0 0 1 1
Answer = (1 1 0 1) 2

8) Find 2'S complement of (1 0 1 0 0 0 1 1) 2

0 1 0 1 1 1 0 0 1 - 1's Complement
+ 1
0 1 0 1 1 1 0 1 0 - 2's complement.

9) Substract 1 1 1 0 0 1 2 from 1 0 1 0 1 1 2 using 2's complement method

1 0 1 0 1 1
+ 0 0 0 1 1 1 - 2's comp. of 1 1 1 0 0 1
1 1 0 0 1 0 in 2's complement form
Answer (0 0 1 1 1 0)2

10) List the different number systems?

i) Decimal Number system
ii) Binary Number system
iii) Octal Number system
iv) Hexadecimal Number system

11) State the abbreviations of ASCII and EBCDIC code?

ASCII- American Standard Code for Information Interchange.
EBCDIC-Extended Binary Coded Decimal Information Code.

12) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction(a) X - Y and (b) Y - X using 1's complements.

a) X - Y = 1010100 - 1000011
X = 1010100
1's complement of Y = + 0111100

Sum = 10010000
End -around carry = + 1

Answer: **X - Y = 0010001**

b) Y - X = 1000011 - 1010100
Y = 1000011
1's complement of X = + 0101011

Sum = + 1101110

13) What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative property and distributive property.

14) State the associative property of boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is statedas follows:
A+ (B+C) = (A+B) +C

15) State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is:
A+B=B+A

16) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the the several variables and then AND ing the sums. The distributive property is:
A+BC= (A+B) (A+C)

17) Simplify the following using De Morgan's theorem [((AB)'C)" D]'

[((AB)'C)" D]' = ((AB)'C)" + D' [(AB)' = A' + B']
= (AB)' C + D'
= (A' + B')C + D'

18) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra.
They are,
1) The complement of a product is equal to the sum of the complements.
(AB)' = A' + B'
2) The complement of a sum term is equal to the product of the complements.
(A + B)' = A'B'

19) Reduce A.A'C

A.A'C = 0.C [A.A' = 1]
= 0

20) Reduce A(A + B)

A(A + B) = AA + AB
= A(1 + B) [1 + B = 1]
= A.

21) Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C
= A'C' + A'BC [A + A' = 1]
= A'(C' + BC)
= A'(C' + B) [A + A'B = A + B]

22) Reduce AB + (AC)' + AB'C(AB + C)

AB + (AC)' + AB'C(AB + C) = AB + (AC)' + AAB'BC + AB'CC
= AB + (AC)' + AB'CC [A.A' = 0]
= AB + (AC)' + AB'C [A.A = 1]
= AB + A' + C' =AB'C [(AB)' = A' + B']
= A' + B + C' + AB'C [A + AB' = A + B]
= A' + B'C + B + C' [A + A'B = A + B]
= A' + B + C' + B'C
=A' + B + C' + B'
=A' + C' + 1
= 1 [A + 1 =1]

23) Simplify the following expression Y = (A + B)(A + C')(B' + C')

Y = (A + B)(A + C')(B' + C')
= (AA' + AC +A'B +BC)(B' + C') [A.A' = 0]
= (AC + A'B + BC)(B' + C')
= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'
= AB'C + A'BC'

24) Show that (X + Y' + XY)(X + Y')(X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X)(X + Y')(X' + Y) [A + A'B = A + B]
= (X + Y')(X + Y')(X'Y) [A + A = 1]
= (X + Y')(X'Y) [A.A = 1]
= X.X' + Y'.X'.Y
= 0 [A.A' = 0]

27) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C + A'BC
=AB + AB'C + A'BC
=A(B + B'C) + A'BC
=A(B + C) + A'BC
=AB + AC + A'BC
=B(A + C) + AC
=AB + BC + AC
=AB + AC +BC ...Proved

28) Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC
=AC(B + B') + AB(C + C') + (A + A')BC
=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC
=ABC + ABC' +AB'C + AB'C' [A + A =1]

29) Define duality property.

Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

30) What are the methods adopted to reduce Boolean function?

i) Karnauh(K map) map
ii) Tabular method or Quine Mc-Cluske

31) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.

32) Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC'

Y = A'B'C' + A'B'C + A'BC + ABC'
=m0 + m1 +m3 +m6
=_m(0, 1, 3, 6)

33) Write the maxterms corresponding to the logical expression
Y = (A + B + C')(A + B' + C')(A' + B' + C)

= (A + B + C')(A + B' + C')(A' + B' + C)
=M1.M3.M6
=_ M(1,3,6)

34) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

35) What is a prime implicant?
A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

38) What is an essential implicant?
If a min term is covered by only one prime implicant, the prime implicant is said to be Essential.

39). What is a Logic gate?
Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

40). Give the classification of logic families

logic families

1. Bipolar 2.Unipolar
1. Saturated 2. Non Saturated 1. PMOS
1.1 RTL 2.1.Schottky TTL 2. NMOS
1.2 ECL 2.2. DTL 3. CMOS
1.3 I I C
1.4 TTL

41). What are the basic digital logic gates?
The three basic logic gates are
1. AND gate
2. OR gate
3. NOT gate
The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

42).Mention the classification of saturated bipolar logic families.
The bipolar logic family is classified as follows:
1. RTL- Resistor Transistor Logic
2. DTL- Diode Transistor logic
3. I2L- Integrated Injection Logic
4. TTL- Transistor Transistor Logic
5. ECL- Emitter Coupled Logic

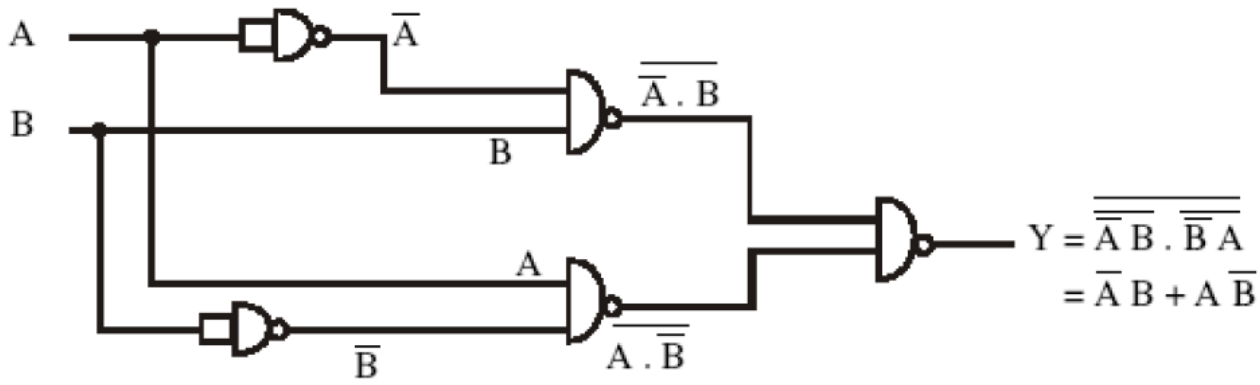
43). Mention the important characteristics of digital IC's?
1. Fan out
2. Power dissipation
3. Propagation Delay
4. Noise Margin
5. Fan In
6. Operating temperature
7. Power supply requirements

44). Define Fan-out?
Fan out specifies the number of standard loads that the output of the gate can drive with out impairment of its normal operation.

45). Define power dissipation?
Power dissipation is measure of power consumed by the gate when fully driven by all its inputs.

46) Define combinational logic
When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic

47)Implement the Boolean Expression for EX – OR gate using NAND Gates.



48)Determine the prime implicants of the function
F (W,X,Y,Z) = (1,4,6,7,8,9,10,11,15)

List all the min terms
Arrange them as per the number of ones based on binary equivalent
Compare one group with another for difference in one and replace the bit with dash.
Continue this until no further grouping possible.
The unchecked terms represent the prime implicants.
F = X'Y'Z + W'XZ' + W'XY + XYZ + WYZ + WX'
Minimum Set of prime implicants F = X'Y'Z + W'XZ' + XYZ + WX'

49) Simplify the Boolean function using K-map.
F(A,B,C,D,E) = (0,2,4,6,9,13,21,23,25,29,31)
Five variables hence two variable k maps one for A = 0 and the other for A = 1.
F = A'B'E' + BD'E + ACE

50) Obtain the canonical sum of products of the function Y = AB + ACD
Y = AB (C + C')(D + D') + ACD (B + B')
Y = ABCD + ABCD' + ABC'D + ABC'D' + AB'CD

51) State the postulates and theorems of Boolean algebra.
X + 0 = X X · 1 = X
X + X' = 1 X · X' = 0
X + X = X X · X = X
X + 1 = 1 X · 0 = 0
(X')' = X
X + Y = Y + X XY = YX
X + (Y + Z) = (X + Y) + Z X(YZ) = (XY)Z
X(Y + Z) = XY + XZ X

52)List the two categories of RAMs.

The two categories of RAMs are static RAM(SRAM) and dynamic RAM (DRAM).
Static RAM uses flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

53). List the two types of SRAM

1. Asynchronous SRAMs
2. Synhronous Burst SRAMs

54)Give the feature of UV EPROM

UV EPROM is electrically programmable by the user, but the store data must be erased by exposure to ultra violet light over a period of several minutes.

55).Give the feature of flash memory.

The ideal memory has high storage capacity, non-volatility; in-system read and write capability, comparatively fast operation. The traditional memory technologies such as ROM,PROM, EEPROM individually exhibits one of these characteristics, but no single technology has all of them except the flash memory.

Flash memories :
They are high density read/write memories that are non-volatile, which means data can be stored indefinitely with out power.
The three major operations in a flash memory are Programming, Read and Erase operation.

57). Define Flip flop.
The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

58)What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are,
RS flip-flop
SR flip-flop
D flip-flop
JK flip-flop
T flip-flop

59). Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called ‘race around condition’.

60). What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop.
The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

61) What is a master-slave flip-flop?
A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

62)Define registers.
A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary
information/number containing n-bits.

63).Define shift registers.
The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

64)What are the different types of shift type?
There are five types. They are,
_ Serial In Serial Out Shift Register
_ Serial In Parallel Out Shift Register
_ Parallel In Serial Out Shift Register
_ Parallel In Parallel Out Shift Register
_ Bidirectional Shift Register

65).Explain the flip-flop excitation tables for RS FF.

RS flip-flop
In RS flip-flop there are four possible transitions from the present state to the
next state. They are,
0 0 transition: This can happen either when R=S=0 or when R=1 and S=0.
0 1 transition: This can happen only when S=1 and R=0.
1 0 transition: This can happen only when S=0 and R=1.
1 1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

66). Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state.
They are,
0 0 transition: This can happen when J=0 and K=1 or K=0.
0 1 transition: This can happen either when J=1 and K=0 or when J=K=1.
1 0 transition: This can happen either when J=0 and K=1 or when J=K=1.
1 1 transition: This can happen when K=0 and J=0 or J=1.

Q. 67 what is VHDL

Ans: VHDL stands for “VHSIC Hardware Description Language.” VHSIC, in turn, stands for “Very High Speed Integrated Circuit,” which was a U.S. Department of Defense program.

Q.68 What are Generics?

Ans: Generics are a way to provide static information to the VHDL program. Immediately after writing entity name, we will mention the generics, this generics will provide the data for entire program. Generics basically allow a design entity to be described so that,for each use of that component,its structure and behavior can be changed by generic values.In general they are used to construct parameterized hardware components.Generics can be of any type.but mostly we will give the timing details there.

E.g. :- generic (width : integer := 7);

Generic is a great asset when you use your design at many places with slight change in the register sizes,input sizes etc. But if the design is very unique then,you need not have generic parameters. Also, Generic’s are synthesizable.

Q 69: Are Verilog/ vhdl concurrent or sequential language in Nature?

Ans: Verilog and VHDL both are concurrent languages. Any hardware descriptive language is concurrent in nature.

Q 70. What is A D-latch

A4: D latch is a device it simply transfers data from input to output when the enable is activated.its used for the forming of d flip flops.

Q.70: Which is the default Delay in VHDL?

Ans: delta delay.

Q71: What Is An Alias And Write Its Syntax?

Ans: Alias is an alternative name assigned to part of an object. alias alias_name : subtype isname

Q72: List Out The Objects Of Vhdl?

Ans: Signal, Variable, Constant.

Q73: List Out The Levels Of Abstractions In Vhdl?

Ans: Data flow level, Structural Level, Behavioral Level.

Q74: What Do We Need To Generate Hardware From Vhdl Model?

Ans: We need following tools

- Simulation tool.
- Synthesis tool.
- Implementation tool.

Q75: How The Signal Acts Within A Process And Outside The Process?

Ans: Signal assignment is concurrent outside the process and sequential within a process.

Q76: What can be the various uses of VHDL ?

Ans: The VHDL language can be used for several goals like –

i) To synthesize digital circuits

ii) To verify and validate digital designs

iii) To generate test vectors to test circuits

iv) To simulate circuits

Q77: What is Synthesis?

Ans: Synthesis represents the transformation of an abstract description into a more detailed descrition. In general, the term “synthesis” is used for the automated transformation of RT level descriptions into gate level representations. This transformation is mainly influenced by the set of basic cells that is available in the target technology. While simple operations like comparisons and either/or decisions are easily mapped to boolean functions, more complex constructs like mathematical operators are mapped to a tool specific macro cell library first. This means that a number of adder, multiplier, etc. architectures are known to the synthesis tool and these designs are treated as if they were designed by the user.

Q78: What is the difference between Concurrent & Sequential Statements ?

Ans: Concurrent statements define interconnected processes and blocks that together describe a design’s overall behavior or structure. They can be grouped using block statement. Groups of blocks can also be partitioned into other blocks. At the same level, a

VHDL component can be connected to define signals within the blocks It is a reference to an entity A process can be a single signal assignment statement or a series of sequential statements (SS) Within a process, procedures and functions can partition the sequential statements

Q79: What are VHDL Subtypes ?

Ans: VHDL subtypes are used to constrain defined types. Constraints take the form of range constraints or index constraints. However, a subtype may include the entire range of the base type. Assignments made to objects that are out of the subtype range generate an error at run time. The syntax and an example of a subtype declaration is shown below :-

SUBTYPE First_ten IS INTEGER RANGE 0 to 9;

Q80: Mention what is the difference between the TTL chips and CMOS chips?

Ans:

TTL Chips	CMOS Chips
• TTL chips for transistor transistor logic. It uses two Bi-polar Junction Transistors in the design of each logic gate • TTL chips can consist of a substantial number of parts like resistors • TTLS chip consumes lot more power especially at rest. A single gate in TTL chip consumes about mW of power • TTL chips can be used in computers	• CMOS stands for Complementary Metal Oxide Semi-conductor. It is also an integrated chip but used field effect transistors in the design • CMOS has greater density for logic gates. In a CMOS chip, single logic gate can comprise of as little as two FETs • CMOS chips consume less power. A single CMOS chip consume about 10nW of power • CMOS chip is used in Mobile phones

Q90: Explain what is a sequential circuit?

Ans: A sequential circuit is a circuit which is created by logic gates such that the required logic at the output depends not only on the current input logic conditions, but also on the sequences past inputs and outputs.

Q91: In Verilog code what does “timescale 1 ns/ 1 ps” signifies?

Ans: In Verilog code, the unit of time is 1 ns and the accuracy/precision will be upto 1ps.

Q92: Explain what is the depletion region?

Ans: When positive voltage is transmitted across Gate, it causes the free holes (positive charge) to be pushed back or repelled from the region of the substrate under the Gate. When these holes are pushed down the substrate, they leave behind a carrier depletion region.

Q93: Explain what is the use of defpararm?

Ans: With the keyword defparam, parameter values can be configured in any module instance in the design.

Q94: Explain what is multiplexer?

Ans: A multiplexer is a combination circuit which selects one of the many input signals and direct to the only output.